MCP2515

MCP2515 Silicon Errata

The functionality of the MCP2515 device is described in the Device Data Sheet (DS20001801**H**), except for the anomalies described below.

1. Module: CAN Module

Under one specific condition, a transmit buffer can become corrupted.

1. A lower priority buffer (as configured via TXBnCTRL.TXP<1:0>) is "pending" transmission (not actually transmitting).
2. A higher priority buffer becomes "pending" during the trigger pulse ($1t_{OSC}$ wide), which starts the transmission of the lower priority buffer.
3. The buffers attempt to reprioritize because the message has not actually started transmission. There is a small window ($1t_{OSC}$ wide) where the buffer has been committed to transmit, but is still viewed as "pending" by the logic. If the higher priority buffer becomes “pending” during this window, the buffers will not reprioritize successfully and corruption will occur.

Work around

There are a few possible work arounds:

- Request-To-Send (RTS) the higher-priority buffer first to avoid the possibility of reprioritization errors.
  This could be implemented as follows:
  Configure Transmit Buffer 2 (TXB2), TXB1, and TXB0 with the same priority. Since all buffers are configured with the same priority, TXB2 will be transmitted first, followed by TXB1 and TXB0.
  Now follow the sequence:
  1) Load the first message to transmit in TXB2 and RTS TXB2.
  2) Load the second message to transmit in TXB1 and RTS TXB1.
  3) Load the third message to transmit in TXB0 and RTS TXB0.
  4) Now wait until TXB0 has transmitted its message, before reloading TXB2. This ensures that all three messages are transmitted in the correct order and the highest priority buffer is always requested first.
  Afterwards, restart the sequence from Step 1.
- RTS of all full buffers at the same time. The internal buffer priority will determine the transmission sequence.
- Send messages one at a time (i.e., check TXnIF before sending the next message).

2. Module: SPI Module

Holding $\overline{CS}$ low for a long time after an SPI command, which initiates a CAN message, may keep the CAN transmit request “pending”, causing the CAN message to be repeated.

Two scenarios:

1. Generating an “SPI RTS” command while in SPI Mode 11 (Mode 00 is not affected): If an “SPI RTS” command is generated and $\overline{CS}$ is held low for longer than it takes for the CAN message to transmit, the message will be transmitted again. This occurs because the SPI module will keep the message “pending” either until it detects a final rising edge on SCK (Mode 11 does not provide this edge) or until $\overline{CS}$ goes high.
2. Generating an “SPI Byte Write” to set the transmit request (TXREQ) bit directly while in either SPI mode: This scenario is the same as the previous, except that the condition will occur in either mode (Mode 00 or Mode 11). This occurs because, for byte writes, the SPI module will release the pending status to the CAN module when $\overline{CS}$ is high.

Work around

There are a few possible solutions:

- Raise $\overline{CS}$ before the CAN message has “completed” transmission, which is an absolute minimum of 47 µs.
- If $\overline{CS}$ cannot be raised in a timely manner (rare), Use the “SPI RTS” command on Mode 00.
- Use hardware pins ($\overline{TXnRTS}$) to request transmission.

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3. Module: Oscillator Module

In silicon revisions prior to revision B2: The oscillator module may continue to operate when the device is placed in Sleep mode if the DC voltage on the OSC1 pin is too low. The rest of the device enters Sleep mode normally. This scenario results in higher-than-specified standby current (I_{DDS}).

Work around

This issue was addressed and no longer occurs in silicon revision B2. See **Appendix B: "Silicon Revision History"** to determine how to identify silicon revision(s) prior to revision B2.

Revision B0 and earlier: Configure the crystal circuit such that the maximum input signal is achieved on the OSC1 pin without overdriving the crystal. This can be accomplished by using crystals that require minimal or no series resistance (R_S), as shown in the crystal circuit diagram of the Device Data Sheet. In addition, matching the capacitors (C1 and C2) may help.

4. Module: RAM Module

In silicon revisions prior to revision B2: Transmit buffer 1 and/or 2 could become corrupted if, while receiving a CAN message, an RTS occurs during the first oscillator cycle of TQ0 of selected bits in the CAN message. This corresponds to the MCP2515's internal CAN clock high time, which is 1 TOSC wide.

Work around

This issue was addressed and no longer occurs in silicon revision B2. See **Appendix B: "Silicon Revision History"** to determine how to identify silicon revision(s) prior to revision B2.

Revision B0 and earlier: If using only one transmit buffer, use buffer 0. Otherwise, to ensure the correct message is transmitted 100% of the time, read the transmit buffer after the successful transmission to verify the contents.

5. Module: CAN Module

In silicon revisions prior to revision B4: Under one condition, the device will make the first five identifier bits all dominant (logic 0) regardless of the value in the transmit buffer ID register.

If the MCP2515 detects a Start-of-Frame (SOF) in the third bit of interframe space and if the MCP2515 is pending transmission of a message, the first five bits of the identifier will become dominant.

Work around

Revision B4 and later: This issue was addressed and no longer occurs in silicon revisions B4 and later. See Appendix B to determine how to identify silicon revisions prior to revision B4.

Revision B2 and earlier: If possible, have the other nodes in the system filter out messages where the first five bits are dominant

Clarifications/Corrections to the Data Sheet:

In the MCP2515 Data Sheet (DS20001801**H**), the following clarifications and corrections should be noted:

None.

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APPENDIX A: REVISION HISTORY

Revision H (January 2018)

- Updated work around for transmit buffer reprioritization in CAN Module

Revision G (March 2007)

- Added SPI Module

Revision F (July 2006)

- Added CAN Module

Revision E (October 2005)

- Updated CAN Module information in this document

Revision D (February 2005)

- Added CAN Module to this document

Revision C (September 2004)

- Added additional information to RAM Module
- Added Oscillator Module to this document

Revision B (May 2004)

- Added RAM Module to this document

Revision A (January 2004)

- Initial release of this document, silicon issue (Oscillator Module)

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APPENDIX B: SILICON REVISION HISTORY

The following table and package marking information indicates how to determine the revision of the MCP2515 device. The revision information can be determined by the Year and Week Code of the manufacturer printed on the device.

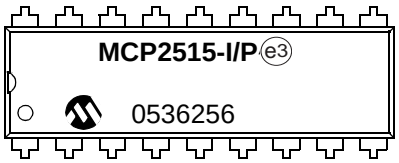
TABLE B-1: SILICON REVISION/DEVICE MARKING

Silicon Revision	YYWWNNN		Comments
	Start Date	End Date	
Rev B4	0538NNN	—	In Production
Rev B2	0450NNN	0537NNN	
Rev B0	—	0449NNN	

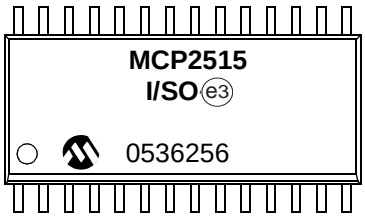
Legend: “N” is any alphanumeric character.

Package Marking Information

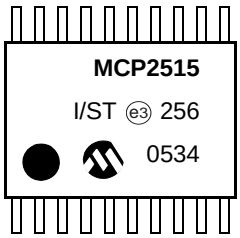
18-Lead PDIP



18-Lead SOIC



20-Lead TSSOP



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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